APPENDIX A: MARKED-UP SPECIFICATION

In the specification:

On page 11, please replace the second full paragraph with the following:

Referring now to FIG. 2D, a masking layer [58] 57 is applied over the top of TEOS layer 56 and vias are formed in the second cap layer 38 in preparation for depositing the upper Cu metal layer 58 including contact regions 42 and 44 and to expose the top surfaces of the upper barrier metal layer 36 and the TaN region 32 over region 16 of the lower Cu metal layer. FIG. 2D shows the structure remaining after the formation of the upper Cu metal layer (including liners 20) but prior to the defination of contact regions 42 and 44 therein as a part of the damascene process.

In the Claims

Kindly amend claims 1, 6 and 10 as follows:

1. (Amended) A metal-to-metal antifuse formed over a lower Cu metal layer planarized with the top surface of a lower insulating layer comprising:

a lower barrier layer disposed over the lower Cu metal layer;

an antifuse material layer disposed over said lower barrier layer;

[An] an upper barrier layer disposed over said antifuse material layer;

an upper insulating layer disposed over said upper barrier layer; and

an upper Cu metal layer planerized with a top surface of the upper insulating layer and having a contact extending therethrough to make electrical contact with said upper barrier.

6. (Amended) The metal-to-metal antifuse of claim 2 wherein said first and second cap layers are formed from [TiN] SiN.

10. (Amended) A method for fabricating a metal-to-metal antifuse comprising:

forming a lower barrier layer over a lower Cu metal layer planarized with the top surface of a lower insulating layer;

forming an antifuse material layer over said lower barrier layer;

forming an upper barrier layer disposed over said antifuse material layer;

forming [An] an upper insulating layer disposed over said upper barrier layer and said antifuse layer;

forming a via in said upper insulating layer to expose a top surface of said upper barrier layer;

forming an upper Cu metal layer over said upper insulating layer and in said via to make electrical contact with said upper barrier layer; and

planarizing a top surface of said upper Cu metal layer and a top surface of said upper insulating layer.